AMENDMENT TO SPECIFICATION

Please delete the word "off" in the specification paragraph on page 3 lines 1 -9. The amended paragraph follows.

It is a further object [[of]] in exemplary embodiments the present invention to provide for a global bitline to be available in every cycle for Read/Write to the different banks, while WriteBack is taking place at yet another different bank at the same time. This is handled by a special "cut-off" device in the PSA which decouples the global bitline from the WriteBack circuit. After a Read cycle, the WriteBack is performed at the local PSA decoupled from the global bitline. The global bitlines are available for Read/Write at a different bank every cycle (while WriteBack is taken place). The decoupling of global bitline from local sense amplifier during WriteBack is key to the performance delivered by the single cycle Read/Write architecture.

Please delete the word "off", and add the word "as", in the specification paragraph from line 15 on page 3 to line 4 on page 4. The amended paragraph follows.

It is a further object [[of]] in exemplary embodiments the invention to teach a new, area efficient PSA which comprise at least two amplification stages, high gain, single ended sensing buffers, feedback circuit for enhanced WriteBack/Write operations and the global bitline isolation "cut-off" device. The Read/Write/WriteBack operations and their controls can be combined area-efficiently in a PSA circuit which can have as few as 6 FET devices. There can be one more NFET per bitline for bitline multiplexing. The two stage buffer arrangement enables the first stage to amplifier a small bitline signal (e.g. 200mV) to almost full Vdd swing (e.g. 1V) to drive the second stage which has enough gate overdrive to handle a long, heavily capacitance loaded global bitline. Such structure results in small sense amplifier FET devices that can drive a long global bitline (GBL) spanning a typical chip (e.g. 10 mm).

Please delete the word "off" in the specification paragraph on page 4 lines 7 - 12. The amended paragraph follows.

Exemplary embodiments of the present invention also teach a linearly growable bank structure with single ended bitline and global bitline which allows each DRAM array (same as bank) to be placed in a linear (vertical) direction on top of each other. In this manner [[of]] all the bits associated with an entire wordline can be read or written to the secondary sense amplifier, and then to the I/O located at the edge of the macro. The global bitlines run over the banks linearly for the Read/Write and I/O operations.

Please replace the whole section of "BRIEF DESCRIPTION OF THE DRAWINGS" commencing on page 5 line 3 with the amended one below.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the present invention will become apparent from the accompanying detailed description and drawings, wherein:

Fig. 1 shows exemplary embodiments of DRAM primary sense amplifiers with data storage and data write-back capability, and two amplification stages;

1A, with grounded first stage amplifier, and feedback device controlled by the output of first stage amplifier;

1B, with source reference bias first stage amplifier, and feedback device controlled by the write-back control signal;

1C, shows a ground sensing scheme, essentially a complementary version of the primary sense amplifier in 1A;

Fig. 2 shows an exemplary embodiment of a DRAM primary sense amplifier with data storage and data write-back capability;

Fig. 3 shows an exemplary embodiment of a DRAM secondary sense amplifier with two amplification stages;

Fig. 4 shows examples of executed operation and timing of the pipelined architecture DRAM;

Fig. 5 shows waveform examples on various nodes of the pipelined architecture DRAM;

5A, shows a Read command and a WriteBack command as executed in the same cycle;

5B, shows a Read command and a WriteBack command as executed in differing cycles;

Fig. 6. shows exemplary embodiments of various modular DRAM size increases;

6A, illustrates a modular increase of I/O size;

6B, illustrates a modular increase of banking size, and combination of banking size and I/O size increase; and

Fig. 7. shows an exemplary floorplan of a two dimensional growable Read/Write/WriteBack DRAM.

Please amend specification paragraph on page 11 lines 3 - 7, as given below.

For a [[A]] representative embodiment the various voltages can be found in TABLE 1, and in the following discussion for data 0 and 1, for Read and Write, on the bitline and other nodes of the circuit. It also shows the design parameter: the source reference voltage (Vref SA), and the NFET threshold (VtSA) of the first stage sense amplifier150. The term "wc" stands for worst case.

Please amend specification paragraph on page 15 lines 9 - 17, as given below.

For the [[The]] PSA embodiments of Fig. 1A and Fig. 1B ~~in the~~ a small PFET 180 is connected to the feedback path 155. The feedback path 155 itself is opened up by passtransistor 156 during Write or WriteBack operations. Fig. 1B shows device 180

controlled by the signal bWB and it is used to hold the feedback path high (VBLH). It may not be needed if the source 170 of the first stage 150 NFET, Vref SA is at GND since then the feedback line can hold up as there is negligible leakage from the second stage 160 NFET during the WriteBack cycle. For a slight variant which is functionally equivalent to the PSA shown in Fig. 1B, in Fig. 1A the gate of the small PFET 180 is controlled by Vsa 190. The source of the first stage 150 NFET is GND in the embodiment shown in Fig. 1A.